[10191/2251]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s)	:	Richard SPITZ et al.
Serial No.	:	To Be Assigned
Filed	:	Herewith
For	:	ARRANGEMENT HAVING P-DOPED AND N-DOPED SEMICONDUCTOR LAYERS, AND METHOD FOR THE MANUFACTURE THEREOF
Examiner	:	To Be Assigned
Art Unit	:	To Be Assigned

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT AND
37 C.F.R. § 1.125 SUBSTITUTE SPECIFICATION STATEMENT

S I R:

Kindly amend the above-captioned application before examination, as set forth below.

IN THE SPECIFICATION AND ABSTRACT:

In accordance with 37 C.F.R. § 1.121(b)(3), a Substitute Specification (including the Abstract, but without claims) accompanies this response. It is respectfully requested that the Substitute Specification (including Abstract) be entered to replace the Specification of record.

IN THE CLAIMS:

On the first page of the claims, first line, change "What is claimed is:" to --WHAT IS CLAIMED IS:--.

Please cancel, without prejudice, claims 1 to 23 in the underlying PCT application.

EL594613635

Please add the following new claims:

24. (New) An arrangement, comprising:

p-doped semiconductor layers;

n-doped semiconductor layers; and

a plurality of transitions arranged between the p-doped semiconductor layers and the n-doped semiconductor layers, the transitions displaying a Zener breakdown upon application of a characteristic voltage for each of the transitions, wherein the characteristic voltages of the transitions additively correspond to a breakdown voltage of the arrangement.

25. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers and the n-doped semiconductor layers are highly doped.

26. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers and the n-doped semiconductor layers exhibit a constant doping.

27. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers and the n-doped semiconductor layers are doped at a same concentration.

28. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers form at least two groups doped at different concentrations.

29. (New) The arrangement according to claim 24, wherein the n-doped semiconductor layers form at least two groups that are doped at different concentrations.

30. (New) The arrangement according to claim 24, further comprising:

an n-doped substrate on which are arranged the p-doped semiconductor layers and the n-doped semiconductor layers.

31. (New) The arrangement according to claim 30, wherein a doping type of a semiconductor layer farthest away from the n-doped substrate corresponds to a doping type of the n-doped substrate.

32. (New) The arrangement according to claim 30, wherein a doping type of a semiconductor layer farthest away from the n-doped substrate is different than a doping type of the n-doped substrate.

33. (New) The arrangement according to claim 30, wherein the n-doped substrate has a thickness of approximately 500μm.

34. (New) The arrangement according to claim 24, further comprising:

a p-doped substrate on which are arranged the p-doped semiconductor layers and the n-doped semiconductor layers.

35. (New) The arrangement according to claim 34, wherein a doping type of a semiconductor layer farthest away from the p-doped substrate corresponds to a doping type of the p-doped substrate.

36. (New) The arrangement according to claim 34, wherein a doping type of a semiconductor layer farthest away from the p-doped substrate is different than a doping type of the p-doped substrate.

37. (New) The arrangement according to claim 35, wherein the p-doped substrate has a thickness of approximately 500μm.

38. (New) The arrangement according to claim 24, wherein the p-doped semiconductor layers and the n-doped semiconductor layers have a thickness of approximately 4μm.

39. (New) The arrangement according to claim 24, wherein a concentration of doping for the p-doped semiconductor layers and the n-doped semiconductor layers is approximately 2×10^{19} atoms/cm^3.

40. (New) The arrangement according to claim 24, wherein ten transitions are provided between the p-doped semiconductor layers and the n-doped semiconductor layers.

41. (New) The arrangement according to claim 24, further comprising:

metal contacts arranged over an entire respective surface of an upper side and a lower side of the arrangement.

42. (New) The arrangement according to claim 24, wherein the n-doped semiconductor layers and the p-doped semiconductor layers are silicon layers.

43. (New) A method to manufacture an arrangement having p-doped semiconductor layers, n-doped semiconductor layers, and transitions arranged between the p-doped semiconductor layers and the n-doped semiconductor layers, the transitions displaying a Zener breakdown upon application of a characteristic voltage for each of the transitions, wherein the characteristic voltages of the transitions additively correspond to a breakdown voltage of the arrangement, the method comprising:

applying the p-doped semiconductor layers and the n-doped semiconductor layers by epitaxy.

44. (New) The method according to claim 43, wherein the epitaxy is applied at approximately 1180°C.

45. (New) The method according to claim 43, wherein the epitaxy is performed at a growth rate of approximately 4 μm/min.

46. (New) The method according to claim 43, further comprising:

sputtering metal contacts onto an upper side and a lower side of the arrangement.

47. (New) The method according to claim 46, further comprising:

after sputtering, dividing the arrangement into individual chips.

48. (New) The method according to claim 47, further comprising:

removing edges of the individual chips.

49. (New) The method according to claim 43, further comprising:

assembling thin silicon discs through wafer bonding.

REMARKS

This Preliminary Amendment cancels, without prejudice, claims 1 to 23 in the underlying PCT Application No. PCT/DE01/02309. This Preliminary Amendment adds new claims 24 to 49. The new claims, inter alia, conform the claims to U.S. Patent and Trademark Office rules and do not add new matter to the application.

In accordance with 37 C.F.R. § 1.121(b)(3), the Substitute Specification (including the Abstract, but without the claims) contains no new matter. The amendments reflected in the Substitute Specification (including Abstract) are to conform the Specification and Abstract to U.S. Patent and Trademark Office rules or to correct informalities. As required by 37 C.F.R. §§ 1.121(b)(3)(iii) and 1.125(b)(2), a Marked-Up Version of the Substitute Specification comparing the Specification of record and the Substitute Specification also accompanies this Preliminary Amendment. Approval and entry of the Substitute Specification (including Abstract) is respectfully requested.

The underlying PCT Application No. PCT/DE01/02309 includes an International Search Report, dated November 5, 2001, a copy of which is included.

It is respectfully submitted that the subject matter of the present application is new, non-obvious and useful. Prompt consideration and allowance of the application are respectfully requested.

Respectfully submitted,

KENYON & KENYON

By. Dorn agent (Reg. No. 41,172)

Dated: 3/5/02

By: Richard L. Mayer

Richard L. Mayer
Reg. No. 22,490
One Broadway
New York, New York 10004
(212) 425-7200

4/pts

[10191/2251]

ARRANGEMENT HAVING P-DOPED AND N-DOPED SEMICONDUCTOR LAYERS, AND METHOD FOR THE MANUFACTURE THEREOF

FIELD OF THE INVENTION

The **present** invention relates to an arrangement having p-doped and n-doped semiconductor layers which exhibits transitions between the p-doped semiconductor layers and n-doped semiconductor layers, the transitions displaying a Zener breakdown upon application of a voltage characteristic of a transition. The **present** invention further concerns a method for manufacturing the arrangement according to the present invention.

[Background of the Invention] BACKGROUND OF THE INVENTION

The use of semiconductor components to limit voltages is known. Zener diodes (Z diodes), in particular, are used for this purpose. If Zener diodes are operated in the blocking or reverse direction, they display a pronounced breakdown behavior at comparatively low breakdown voltages. The value of the breakdown voltage of a diode depends substantially on the doping concentration of the semiconductor material. In highly doped diodes, a very narrow barrier layer forms, so that high electrical field strengths above the p-n transition are present upon application of even small reverse voltages.

If the field strength exceeds a value [on the order of] **of approximately** 10^6 V/cm, valence electrons in the vicinity of the almost charge-carrier-free p-n transition can be pulled out of their bonds. In the band model, this effect is represented as tunneling through the forbidden band. At low voltages below the breakdown voltage (also called the Zener voltage), only the (usually negligibly low) reverse current flows. When the Zener voltage is reached, the current rises sharply due to charge carrier emission, thus preventing any further increase in voltage. At breakdown voltages below 4.5 V, the result is a "pure Zener" breakdown. At higher breakdown voltages there is another competing breakdown effect, namely the so-called avalanche breakdown. This predominates at voltages above 7 V, and results substantially from avalanching impact ionizations in the semiconductor. Because of

EL594613635

Marked-Up Version of the Substitute Specification

its defined and reversible breakdown, a Zener diode is suitable as a voltage limiter. If two Zener diodes are connected together in anti-serial fashion, i.e. in series but with opposite polarity, symmetrical breakdown behavior will be obtained.

A circuit of this kind is [depicted] **illustrated** in Figure 6, which depicts a first Zener diode 110 and a second Zener diode 112 connected anti-serially. Arrangements of this kind are used for voltage limiting in order to limit both polarities of a voltage applied to contacts 114, 116.

Figure 7 shows the corresponding current/voltage characteristic of the circuit depicted in Figure 6. In the diagram of Figure 7[.], the current flowing through Zener diodes 110, 112 is plotted against the voltage applied to contacts 114, 116. Ignoring path resistances and the rise in breakdown voltage resulting from self-heating, the breakdown voltage of the arrangement is UZ1 + UF, where UZ1 denotes the breakdown voltage of one of the Zener diodes (which in the present case are assumed to be identical) and UF is the voltage drop of a diode in the forward direction. If a voltage limiting circuit of this kind is to be designed for higher limit voltages, however, the positive breakdown voltage temperature response, **as** seen in Figure 7, occurs. In Figure 7, a solid line shows a characteristic at room temperature (RT) and a dashed line shows a characteristic at much higher temperature (HT). The positive temperature response seen here results principally from the fact that in diodes designed for higher breakdown voltages, avalanche breakdown is predominant.

The temperature dependence of the characteristic shown in Figure 7 is undesirable. The voltage limiting circuit of Figure 6 additionally has the disadvantage that two separate components are needed to implement it, entailing additional circuit complexity.

[Advantages of the Invention

The invention expands upon the arrangement of the species according to Claim 1 by the fact that]

SUMMARY OF THE INVENTION

In an example embodiment of the present invention a plurality of transitions between p-doped semiconductor layers and n-doped semiconductor layers are present; and [that the] characteristic voltages additively make up [the]**a** breakdown voltage of the entire arrangement. [It is thus] **Through the present invention it is** no longer necessary to use two separate components to bring about voltage limitation for both polarities of the voltage._ Instead, a single arrangement having multiple transitions between p-doped semiconductor layers and n-doped semiconductor layers [can provide]**provides** voltage limitation for both polarities. Since the characteristic voltages of the transitions at which the transitions exhibit a Zener breakdown moreover additively make up the breakdown voltage of the entire arrangement, it is possible to select a low level for the individual breakdown voltages and nevertheless, because of the addition of the individual breakdown voltages, effect limitation to a comparatively high voltage. _Since the Zener effect greatly predominates at the small characteristic voltages of the individual transitions (which for example can be 4.2 V), (i.e. avalanche breakdown still plays no role or only a [greatly]subordinate role), a practically temperature-independent characteristic curve [can]**may** be made available despite the high limit voltage that is provided.

[Preferably the]**The** semiconductor layers [are]**may be** highly doped. A high level of doping results in a low breakdown voltage and thus, in the desired temperature, independence of the apparatus.

[It may be advantageous if the]**The** semiconductor layers **may** exhibit constant doping[. This is advantageous in the interest of] **allowing** simple manufacture. With constant doping the breakdown voltage is moreover [easy to calculate]**calculable** because of the identical properties of the transitions between layers.

[It may also be preferred if the]**Another embodiment provides** p-doped semiconductor layers and n-doped semiconductor layers **which** are doped at the same concentration. This results in a uniform configuration of the depletion zone in both the n-doped semiconductor layers and the p-doped semiconductor layers. This allows the layer sequence to be configured uniformly.

[It may be preferred]**Another embodiment provides** for the p-doped semiconductor layers to form at least two groups that are doped at different concentrations. This

makes it possible to obtain a characteristic that is asymmetrical with respect to voltage polarity, unlike the case of uniform doping of all p- semiconductor layers and all n- semiconductor layers, which yields a symmetrical characteristic. Voltage limitations that differ depending on the polarity of the voltage can thus be made available.

For the same reason, [it may be advantageous if the]**another embodiment provides** n-doped semiconductor layers **to** form at least two groups that are doped at different concentrations.

[It is possible]**Another embodiment provides** for the semiconductor layers to be arranged on an n-doped substrate.

[It is also possible]**Another embodiment provides** for the semiconductor layers to be arranged on a p-doped substrate. [There]**In this embodiment there** is [thus]no dependence on a specific doping of the substrate, thereby making the arrangement flexible in terms of manufacture and utilization.

[It may be useful for the]**The** doping type of the semiconductor layer farthest away from the substrate [to]**may** correspond to the doping type of the substrate.

[On the other hand, however, it is also possible for the]**The** doping type of the semiconductor layer farthest away from the substrate [to]**may** be different from the doping type of the substrate[. Here again, therefore, there is] **providing** flexibility in terms of the manufacture and field of application of the arrangement, and no limitation to a specific doping type for the outermost semiconductor layers.

[It may be advantageous if the]**The** semiconductor layers **may** have a thickness of approximately 4 µm. Such a thickness is suitable, i.e. sufficiently thick, in the context of the feasible breakthrough voltages of the individual transitions and the depletion zone thicknesses related thereto. The [appropriate]thickness prevents the minority charge carriers injected through the transitions polarized in the forward direction from reaching a space charge zone of an adjacent transition that is reverse-polarized. [This is absolutely necessary, since otherwise the] **The** entire arrangement would "fire" (thyristor effect)[.It may be useful] if [the]**not designed in**

this way.

The substrate [has]**may have** a thickness of approximately 500 μm. A substrate thickness on this order ensures, inter alia, sufficient mechanical stability.

The doping concentration [is preferably]**may be provided** in the region of 2 x 10^{19} atoms/cm^3. At such a high doping concentration, a Zener effect is obtained in each transition at the desired low Zener voltage, and thus with a correspondingly low temperature dependence.

In a specific embodiment, approximately ten transitions between p-doped semiconductor layers and n-doped semiconductor layers are provided. At Zener voltages in the region of 4.2 V and conducting voltages in the region of 0.7, an overall breakdown voltage of, for example, 50 V is obtained, without significant temperature dependence. If this level of voltage limitation were to be implemented with a conventional design[according to the existing art], i.e. with individual Zener diodes, the overwhelming dominance of the avalanche effect would result in a considerable and in some cases intolerable temperature dependence.

The arrangement [preferably has]**may have** on its upper side and lower side respective metal contacts which extend over their entire surface. The arrangement is thereby prepared for the further processing that is usually performed on semiconductor components.

The semiconductor layers [are preferably]**may be** silicon layers. The high doping levels and the desired layer structure [can]**may** be brought about [with particular advantage] using silicon.

[According to Claim 17, the] **The present** invention further relates to a method for manufacturing an arrangement having p-doped and n-doped semiconductor layers which exhibits transitions between the p-doped semiconductor layers and n-doped semiconductor layers, the transitions displaying a Zener breakdown upon application of a voltage characteristic of a transition, a plurality of transitions between p-doped semiconductor layers and n-doped semiconductor layers being present, and the characteristic voltages additively making up the breakdown voltage of the entire

arrangement, the method comprising application of the semiconductor layers by epitaxy. Epitaxy [is]**provides** a[particularly] suitable method for building up layer arrangements that constitute the present invention.

The epitaxy [preferably takes]**may take** place at approximately 1180°C. This temperature [has proven particularly favorable for]**allows** defect-free layer formation.

[It is also useful if the]**The** epitaxy [is]**may be** performed at a growth rate of approximately 4 µm/min. This **rate** ensures a high-quality layer structure with a sufficiently rapid manufacturing method.

Metal contacts [are preferably]**may be** sputtered onto the upper side and lower side of the arrangement. By way of these metal contacts, which [preferably]**may** cover the entire upper side and the entire lower side of the arrangement, the arrangement is prepared for further processing. The sputtering method has proven particularly reliable for the application of thin metal layers.

[Preferably the]**The** arrangement [is]**may be** divided into individual chips after the metal contacts are sputtered on. For example, a silicon substrate that is initially used [could]**may** have a diameter of 125 mm. The chips resulting from the method, which are produced, for example, with the use of a circular saw, [can]**may** then have a surface area of, for example, 20 mm^2.

[It is particularly preferable for the]**The** edges of the chips [to]**may** be removed. If the chips are produced, for example, by a sawing operation, crystal disruptions that have a negative effect on the electrical properties of the component are created at the chip edge. This disrupted semiconductor region at the chip edge is then removed, for example to a depth of 50 µm. This can be achieved, for example, by etching in KOH. Etching is often performed[only] after the chip has been soldered at its front and rear sides into a copper housing. Further packaging is then performed in a manner common in diode technology.

In addition to construction of the layer arrangement by epitaxy, [it is also possible to assemble]thin silicon disks **may be assembled** by wafer bonding. Variability thus exists in terms of manufacture.

[The basis of the invention is the surprising recognition that with]**With** a corresponding layer arrangement made up of p-doped and n-doped semiconductor layers, [it is possible to make available]bipolar voltage limitation **are available** with negligible temperature dependence. The breakdown voltage of individual p-n transitions [can]**may** be selected, [by way of]**through** appropriate doping, so that practically only Zener breakdown occurs. Because the layer arrangement is configured in such a way that the breakdown voltages of the individual p-n transitions additively make up the breakdown voltage of the overall arrangement, voltage limitation [can]**may** be achieved even for high voltages with a low temperature dependence.

[Drawings

The invention will be explained below by way of example, with reference to the accompanying drawings and on the basis of embodiments.]

BRIEF DESCRIPTION OF THE DRAWINGS

[Figure 1 schematically shows] **Figure 1 is** a cross [section]**sectional view** of an arrangement according to the present invention[;].

Figure 2 [shows]**is** a characteristic curve of an arrangement as shown in Figure 1[;].

Figure 3 [shows]**is** a doping profile of an arrangement as shown in Figure 1[;].

Figure 4 [schematically shows]**is** a cross [section]**sectional view** of a further embodiment of an arrangement according to the present invention[;].

Figure 5 [shows]**is** a characteristic curve of an arrangement as shown in Figure 4[;].

Figure 6 [shows]**is a schematic layout of** a circuit according to the existing art[;].

Figure 7 [shows]**is** a characteristic curve of the arrangement as shown in Figure 6.

[Description of the Exemplary Embodiments]**DETAILED DESCRIPTION**

Figure 1 schematically shows a cross section of an arrangement according to the present invention. A plurality of p-doped semiconductor layers 12 and n-doped semiconductor layers 14 are arranged on an n-doped silicon substrate 10. A plurality of semiconductor transitions are present between p-doped semiconductor layers 12 and n-doped semiconductor layers 14. P-doped semiconductor layers 12 have a thickness TP, while n-doped semiconductor layers have a thickness TN. In the present case, thicknesses TP and TN are approximately identical and are approximately 4 µm. The substrate has a thickness TS of approx. 525 µm in the present example. Since a total of ten p-doped semiconductor layers and ten n-doped semiconductor layers 14 are arranged on substrate 10, the total thickness T of the arrangement resulting from these data is 605 µm. In the present example, silicon is selected as the semiconductor. Located on n-doped substrate 10 and the uppermost semiconductor layer, which in the present case is an n-doped semiconductor layer 14, are metal contacts 16, 18 that were applied with a sputtering procedure. Semiconductor layers 12, 14 each have a constant doping level of approx. 2×10^{19} atoms/cm^3. Layers 12, 14 were applied by epitaxy onto the respective layer beneath. In [a preferred]**an example** embodiment, the epitaxy takes place in such a way that a temperature of 1180°C and a growth rate of 4 µm/min is selected. In the present example as shown in Figure 1, the layer arrangement is selected [in such a way]that the uppermost layer and bottommost layer (substrate) have the same doping type, in the present case n-doping. [It is also possible for the] **The** two outer semiconductor layers [to]**may also** exhibit p-doping. The outer layers [can moreover]**may** have different doping types, in the context of both an n-type substrate and a p-type substrate.

Figure 2 shows in simplified fashion a characteristic curve of the arrangement shown in Figure 1. If a voltage U that is positive as compared to electrode 16 is applied to metal electrode 18, no current (other than a [relatively low]reverse current) flows until reverse voltage UZ is reached. If an attempt is made to increase voltage U even further, the current through the arrangement rises sharply as a result of the Zener breakdowns at the individual transitions between the semiconductor layers. Since the arrangement is symmetrically constructed, reversing the polarity of the applied voltage U results in the same electrical behavior with the opposite sign. Assuming n p-doped epitaxial layers and [n] n-doped epitaxial layers, the equation for the breakdown voltage UZ is:

$$UZ = n * (UZ1 + UF)$$

where UZ1 is the breakdown voltage of an individual transition, and UF is the forward voltage of an individual p-n diode. The solid line in Figure 2 shows the current/voltage behavior of the arrangement at room temperature (RT). The dashed line shows the behavior at [much]higher [temperature]**temperatures** (HT). [It is evident that until] **Until** very high currents are reached, temperature has practically no influence on the curve. Only at very high current densities, approximately in the region above 200 A/cm^2, is a non-negligible positive temperature coefficient once again present.

Figure 3 depicts the doping profile of the arrangement shown in Figure 1, the number density of doping atoms N being plotted against location x. The solid lines denote n-doped silicon, and the dashed lines denote p-doped silicon. The left side of the diagram in Figure 3 corresponds to the n-doped silicon layer of Figure 1 that is adjacent to metal electrode 18, while the right side of the diagram in Figure 3 corresponds to substrate 10 in Figure 1 that is adjacent to metal electrode 16 of Figure 1. [It is evident that a] **A** constant doping concentration of 2 x 10^{19} atoms/cm^3 is present.

Figure 4 schematically shows a cross section of a further embodiment of an arrangement according to the present invention that [also]results in voltage limitation regardless of the voltage polarity. [It has been mentioned that] **As previously stated,** the arrangement shown in Figure 1 has a characteristic curve that is symmetrical in terms of the polarity of the applied voltage. The arrangement depicted in Figure 4, [on the other hand]**however**, yields an asymmetrical characteristic curve. The particular feature of this arrangement is[the fact] that two types of p-doped semiconductor layers are present. A first p-doped semiconductor layer 20 has a lower doping concentration than a second p+-doped semiconductor layer 22. The doping concentration of the n-type semiconductor layers is uniform. This yields diodes having different breakdown voltages, corresponding to the n-(p+p) and (p+p)-n transitions. When the diodes are loaded in the reverse direction, the breakdown voltage UZ1 of the (p+p)n diode is greater than the breakdown voltage UZ2 of the n(p+p) diode. Assuming n transitions, a voltage at metal contact 18 that is positive with respect to metal contact 16 results in a breakdown voltage

UZ = n * (UZ2 + UF).

If the polarity of the voltage is reversed, the resulting breakdown voltage is

UZ = -n * (UZ1 + UF).

The arrangement shown in Figure 4 is [once again]variable in principle in terms of the outermost semiconductor layers and in terms of doping types. For example, a p-type substrate can also be used instead of an n-type substrate. In the case of a p-type substrate, more highly doped n+-type layers and less highly doped n-type layers would correspondingly be used. The outermost layers of the semiconductor arrangement can in turn be identical or different in terms of doping type.

Figure 5 shows a characteristic curve of an arrangement as shown in Figure 4. With suitable dimensioning in terms of both geometry and concentrations, the result is [once again]practically temperature-independent characteristic curves as depicted in Figure 5. Figure 5 corresponds in [its]**a** general configuration to Figure 2, [although]**while using** the asymmetrical curve[is the critical factor here].

The description above of the exemplary embodiments of the present invention is provided for illustrative purposes only, and not for purposes of limiting the invention. A variety of changes and modifications are possible in the context of the **present** invention without departing from the scope of the invention or its equivalents.

[Abstract]

ABSTRACT OF THE DISCLOSURE

[The invention relates to an] **An** arrangement having p-doped semiconductor layers [(12, 20, 22)]and n-doped semiconductor layers[(14, 10)] which exhibits transitions between the p-doped semiconductor layers [(12, 20, 22)]and n-doped semiconductor layers[(14, 10)], the transitions displaying a Zener breakdown upon application of a voltage characteristic of a transition, a plurality of transitions between p-doped semiconductor layers [(12, 20, 22)]and n-doped semiconductor layers[(14, 10)] being present, and the characteristic voltages additively make up the breakdown voltage of the entire arrangement. [The invention further concerns] **Also described is** a method for manufacturing [an] **the** arrangement [according to the present invention].